Paper / Subject Code: 32207 / Elective - I Finite Automata Theory

T.E. (EXTC) (Sem-V) (C.B.S) Date - 27/11/19

(3 Hours) **Total Marks: 80**

Note the following instructions.

1. Question **No.1** is **compulsory**
2. Attempt **any three** questions from remaining **five questions**
3. **Solve** in **total 4** questions
4. Assume suitable data wherever necessary, justify the same
5. **Figures** to the **right** indicate **full marks.**

1.a Identify the following function is symmetric and expressed it. **[5]**

$f(x, y, z) = \sum(1,2,4,7)$

1.b What are the merits and limitations of Threshold gates? **[5]**

1.c What is the procedure of state minimization using merger methods? **[5]**

1.d Differentiate between Mealy and Moor type state machine. **[5]**

2.a Use the Quine–McCluskey method to obtain the minimal expressions for the following functions. **[10]**

$T(v, w, x, y, z) = \sum(0,1,2,8,9,15,17,21,24,25,27,31)$

2.b Explain the synthesis procedure with suitable example for the design of fundamental-mode asynchronous sequential circuits. **[10]**

3.a Use the map method to generate all prime implicants and indicate which are essential; and obtain the minimal expressions for the following functions. **[10]**

$T(w, x, y, z) = \sum(0,1,2,3,4,6,7,8,9,11,15)$

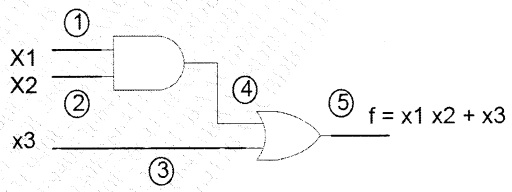
3.b Explain the basic principle of one dimensional path sensitization method. **[06]**

3.c Discuss Possible strategies in Fault Tolerant Design **[04]**

4.a Show that threshold logic realization of Full Adder requires only two threshold elements.(Note that both sum and carry must be generated) **[10]**

4.b Design a modulo 8-binary counter uing T flip-flops. **[10]**

5.a Find the fault table for all stuck-at faults of the following circuit **[10]**



5.b Explain in details, how to identify unknown sequential machine experimentally? **[10]**

6. a Explain the lattice of closed partitions of machine. **[10]**

6. b Draw and explian the ASM chart for a 2-bit inary counter. **[10]**

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