**Q. P. Code: 27582**

**(3 Hours)** **80 Marks**

N.B.: (1) Question No. **1 is compulsory**.

(2) Solve any **three questions** from the **remaining five**

(3) Figures to the right indicate full marks

(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 a) Perform the following operation using 2's compliment [20]

i) $(14)_{10} - (24)_{10}$

ii) $(24)_{10} - (14)_{10}$

Comment on results of (i) and (ii)

b) If $F(A,B,C) = \sum m(0,3,5,7)$ with its truth table and express F in SOP and POS form

c) Compare FPGA and CPLD.

d) Explain Static RAM

Q.2 a) Write VHDL code for 3 bit up counter. [10]

b) Minimize the following expression using Quine McClusky Technique [10]

$F(A,B,C,D) = \sum m(1,3,7,9,10,11,13,15)$

Q.3 a) Design 3 bit Binary to Gray code Converter [10]

b) Draw and explain a neat circuit diagram of BCD adder [10]

Q.4 a) Draw and explain two input TTL NAND gate. [5]

b) Compare combinational circuits and sequential circuits [5]

c) Explain Full Adder circuit using PLA having three inputs, 8 product terms and two outputs. [10]

Q.5 a) What is excitation table? Explain the excitation table of SR flip flop. [5]

b). Convert D flip flop to T flip flop. [5]

c) Draw and explain 3 bit asynchronous binary counter using positive edge triggered JK flip flop. Draw the waveforms. [10]

Q.6 a) Implement following Boolean function using 8:1 multiplexer [6]

$F(A,B,C,D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$

b) State and prove Demorgan's theorem [4]

c) What are shift registers? How are they classified? Explain working of any one type of shift register. [10]

**********