(3 Hours) **Max. marks: 80**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions. [20]

a) Explain bleeder resistor and critical inductance
b) Draw and explain small signal model of FET
c) Explain VI characteristics of PN junction diode
d) State and explain Millers Theorem
e) Why should RC be as large as possible in the design of CE amplifier?
f) Design a self bias circuit using JFET for I_D=3mA, V_{DD}=20V, V_{DS}=0.6V_{DD} (I_{DSS}=8mA, Vp= - 4V)

Q.2 a) Given the information in the circuit diagram Fig. 2(b) determine [05]
(a) Ic (b) R_C and (c) R_B

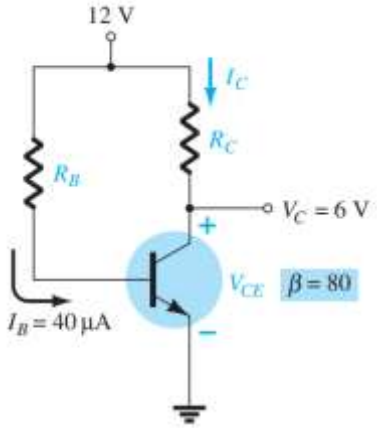

Fig. 2 (b)

b) Define stability factor (S) and explain factors affecting S.Derive the expression for stability factor of collector to base bias circuit [10]

c) For JFET is IDSS = 6mA , Vp= -6V, rd= □, Cgd = 4pF, Cgs = 6pF, Cds=1pF,. Determine VGSQ, IDQ, gmo, gm and midband voltage gain Av [05]

Q.3 a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6)$ mA and $A_V = 12$. [10]

b) Draw CS JFET amplifier with self bias circuit and derive the expression for voltage gain, input impedance and output impedance [10]

Q.4 a) Explain concept of shunt zener regulator. For the shunt zener regulator giving output voltage of 10 V and load resistance varying from 5KΩ to 10KΩ, Vin is varying between 18V to 22V. Find Rs, Pzmax, Sv and Ro. Assume Rz = 4Ω and Izmin = 50μA [10]

b) For the circuit shown below in Fig. 4(b), the transistor parameters are VBE(on) = 0.7V, β=200, VA= □ [10]

i) Derive the expression for lower cutoff frequency (or time constant) due to input coupling capacitor

ii) Determine lower cutoff frequency and midband voltage gain

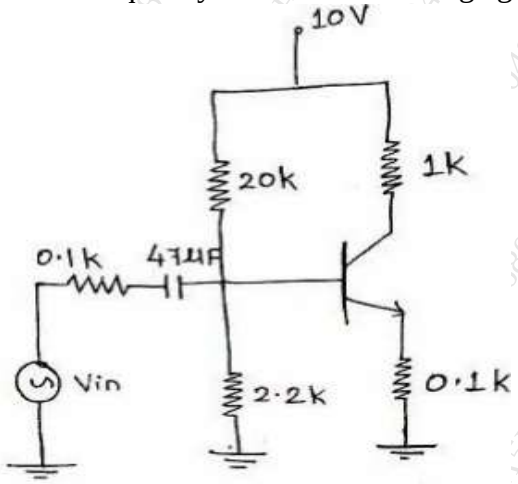

Fig. 4(b)

Q.5 A) A full wave rectifier using a centre tapped transformer with two diodes gives output of 250V and current is 100 +/- 25mA. If the ripple factor is 0.001, Calculate the specification of the devices and components required if the filter used is LC filter [10]

B) Explain effect of bypass capacitor and coupling capacitors on frequency response of amplifier [5]

C) Determine small signal voltage gain of the circuit shown below in Fig 5(c) using hybrid-π model. (β=100,V_A=100V,I_{CQ}=0.95m A) [5]

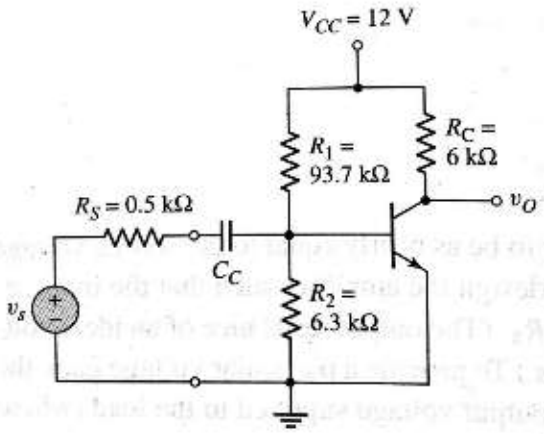

Fig 5(c)

Q.6 Short notes on: (Attempt any four) [20]

a) Small Signal model of diode
b) Zero temperature drift biasing in JFET amplifier
c) Explain different types of filters
d) High frequency hybrid pi equivalent model of CE BJT
e) Comparison of BJT CE and JFET CS amplifier

Transistor type	P_{tot} max @ 25°C Watts	$I_{C(max)}$ @ 25°C Amps	V_{CE} (sat) volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Min) volts d.c.	V_{EBO} (Min) volts d.c.	V_{CEO} volts d.c.	V_{EBO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal min.	typ.	h_{fe} max.	V_{BE} max.	θ_{j-amb} °C/W	Derate above 25°C W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
ECN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	115	1·5	3·5	0·4
ECN 149	30·0	4·0	1·0	50	40	—	—	4	150	30	50	110	35	60	115	1·2	4·0	0·3
ECN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	0·03
BCT147A	0·25	0·1	0·35	50	45	50	—	6	175	115	180	220	125	220	260	0·9	—	—
2N 1132(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	—
BCT148	0·25	0·1	0·35	50	45	50	—	6	175	200	290	450	240	330	500	0·9	—	—

Transistor type	h_{ie}	h_{oe}	h_{re}	θ_{ja}
BC 147A	2·7 KΩ	18μ Ω	$1·5 \times 10^{-4}$	0·4°C/mw
2N 525 (PNP)	1·4 KΩ	25μ Ω	$3·2 \times 10^{-4}$	—
BC 147B	4·5 KΩ	30μ Ω	2×10^{-4}	0·4°C/mw
ECN 100	500 Ω	—	—	—
ECN 149	250 Ω	—	—	—
ECN 055	100 Ω	—	—	—
2N 3055	25 Ω	—	—	—

BFW 11—JFET MUTUAL CHARACTERISTICS

-V_{GS} volts	3·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
I_{DSS} max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·5	0·0
I_{DSS} typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·1	0·2	0·0	0·0	0·0	0·0
I_{DSS} min. mA	4·0	3·0	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel JFET

Type	V_{DS} max. Volts	V_{GS} max. Volts	V_{GS} max. Volts	P_{tot} max. @25°C	T_j max.	I_{DSS}	I_{DSS} (typical)	$-V_p$ Volts	r_d	Above 25°C	θ_{ja}
2N5823	50	50	50	300 mW	175°C	2 mA	3000 μ Ω	6	50 KΩ	2 mW/°C	0·33°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ Ω	2·5	50 KΩ	—	0·33° C/mW

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