## Paper / Subject Code: 50924 / Digital Logic & Computer Architecture

		(5 flours) Total Marks:	00
N.B		1. Question No. 1 is compulsory	
		2. Attempt any <b>three</b> questions from remaining five questions	
		3. Assume suitable data if <b>necessary</b> and justify the assumptions 4. Figures to the <b>right</b> indicate full marks	
Q1	A	Convert	05
		i) 123 in to binary	
		ii) (AB9) <sub>16</sub> in to Decimal iii) (351) <sub>8</sub> in to decimal	
		iv) 129 in to BCD	
		v) 64 in to gray code	
	D	Duran the single and double resision for at for a succession flection of int number	05
	В	Draw the single and double precision format for representing floating point number using IEEE 754 standards and explain the various fields	05
Ω1	C	Explain SR Flip Flop	05
	D	Differentiate between Hardwired control unit and Micro programmed control unit	05
Q2	A	Draw the flow chart of Booths algorithm for signed multiplication and Perform	10
	SV	5 x 2 using booths algorithm	
	В	Explain the different addressing modes.	10
9			
Q3	A	For 132.65 obtain the IEEE 754 standards of Single precision and Double precision format	10
	В	Explain Micro instruction format and write a microprogram for the instruction	10
		$ADD R_1, R_2$	
Q4	A	Consider a 4-way set associative mapped cache with block size 4 KB. The size of the	10
		main memory is 16 GB and there are 10 bits in the tag. Find- 1. Size of cache memory	
		2. Tag directory size	
	ъ		10
	В	Explain Flynn's classification	10
Q5		Explain different types Distributed and Centralized bus arbitration methods	10
Q3	В	Describe the detailed Von-Neumann Model with a neat block diagram	05
	Б		
	C	Describe the characteristics of Memory.	05
Q6		Write Short notes on	20
		a) Grey code, BCD, Excess-3 Code with example	
		b) Encoder and Decoder	
		c) Cache coherence	
		d) Instruction Pipelining	

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