(3 hours) **Total Marks: 80**

N.B. 1. Question **No. 1** is compulsory
2. Attempt any **three** questions from remaining five questions
3. Assume suitable data if **necessary** and justify the assumptions
4. Figures to the **right** indicate full marks

Q1	A	Explain Von Neumann's architecture.	**05**
	B	Draw flow chart of Booths algorithm.	**05**
	C	What is Programmed I/O?	**05**
	D	Explain various pipeline hazards with example.	**05**
	E	Explain IEEE 754 floating point number representation	**05**
Q2	A	Explain set associative cache mapping technique with example.	**10**
	B	What is bus arbitration? Explain any two techniques of bus arbitration.	**10**
Q3	A	Explain various characteristics of memory.	**10**
	B	Using Booths algorithm show the multiplication of -3 * -7.	**10**
Q4	A	Differentiate between Paging and Segmentation.	**10**
	B	Describe the register organization within CPU.	**10**
Q5	A	Explain Flynn's classification.	**10**
	B	Explain the concept of Nano programming.	**10**
Q6	A	What is TLB? Explain working of TLB.	**10**
	B	Explain the concept of Superscalar architecture.	**10**