S.E. (IT) (Sem-III) (CBCGS) (R-2016)

Logic Design

University of Mumbai

Examinations Summer 2022

Time: 2 hour 30 minutes | Max. Marks: 80

Q1. Choose the correct option for following questions. All the Questions are compulsory and carry equal marks

1. What is the ideal value of I_C and V_{CE} respectively for BJT Common Emitter biased circuit operated in cut-off region?

Option A: 0 & V_{CC}
Option B: $I_{C(sat)}$ and V_{CC}
Option C: $I_{C(sat)}$ and 0
Option D: 0 and 0

2. The 2's complement of 1000 is

Option A: 0111
Option B: 1000
Option C: 1001
Option D: 1010

3. BCD equivalent to Decimal $(976)_{10}$ is

Option A: 100011001110
Option B: 001001110110
Option C: 110010110111
Option D: 100101110110

4. The Boolean expression B+AB' is equal to

Option A: A
Option B: B'+A
Option C: A'+B
Option D: A+B

5. Output will be a LOW for any case when one or more inputs are high for a(n):

Option A: OR gate
Option B: NAND gate
Option C: AND gate
Option D: NOR gate

6. For the full adder, assume the input bits are A = 1 (MSB), B = 0, Bin = 1(LSB). The Sum (S) and Carry (Cout) outputs will be

Option A: 0 and 1 respectively
Option B: 0 and 0 respectively
Option C: 1 and 0 respectively
Option D: 1 and 1 respectively

7. 1:8 De-multiplexer has

Option A: 1 input, 8 output and 3 selection lines
Option B: 1 input and 8 output
Option C: 8 input, 1 output and 3 selection lines
Option D: 8 input and 1 output

8. Which of the following is a sequential logic circuit?

Option A: Multiplexer
Option B: Decoder
Option C: Code converter
Option D: Shift Register

9. Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?

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Option A: The Q output is ALWAYS identical to the CLK input if the D input is HIGH
Option B: The logic level at the D input is transferred to output Q on Negative edge of CLK
Option C: The logic level at the D input is transferred to output Q on Positive edge of CLK
Option D: The Q output is ALWAYS identical to the D input if the CLK input is LOW

10. Which design unit is used to describe the internal view (functionality) of the digital hardware in VHDL?
Option A: Entity Declaration
Option B: Architecture Body
Option C: Process Statement
Option D: Signal Assignment Statement

Q2 **Answer any Four questions from the following.** **(5 marks each)**

A Compare three modes of transistor operation based on biasing conditions of each junction and their major application.
B Covert binary number $(10001010)_2$ to decimal, octal, hexadecimal and gray code.
C (i) For the logic circuit shown in Figure 1, write a Boolean expression for output X in terms of inputs. (ii) Convert the Boolean expression for output X into the standard SOP form and write a truth table.

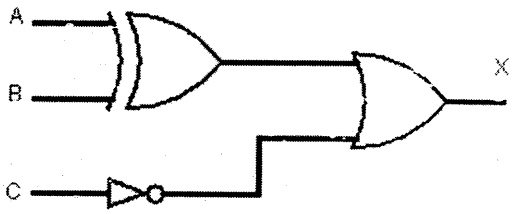

Figure 1

D With neat circuit diagram and truth table explain 2:4 decoder.
E Draw circuit diagram of negative edge triggered T flip-flop and write its function table.
F Explain entity declaration in VHDL.

Q3 **Answer any Four questions from the following.** **(5 marks each)**

A Perform the following arithmetic.
(i) $(1010001)_2 - (1101111)_2$ using 2's complement method.
(ii) $(01011001)_{BCD} + (10010101)_{BCD}$
B With neat diagram explain the working of current mirror circuit.
C Simplify the following equation using Boolean algebra and design simplified function using basic logic gates.

$$F(A,B,C,D) = \bar{A}\,B(\bar{D}+C) + (A + \bar{A}C\bar{D})B$$

D Implement the following logic function using a 4:1 MUX.
$F(A,B,C) = \prod M(0,1,4,7)$
E With neat diagram explain working of 2-bit serial in serial out shift right register using positive edge triggered D Flip-flop.
F Write a VHDL Program for half adder circuit.

Q4.
A **Answer any Two questions from the following.** **(5 marks each)**
i. Convert JK flip-flop to T flip-flop.
ii. Get the Minimum SOP form for the following logic function using Karnaugh Map.
F(A, B, C, D) = Σm(0, 2, 4, 6, 8, 10)
iii. Derive the equation relating CB current gain (α) and CE current gain (β).

B **Answer any One question from the following.** **(10 marks each)**

i. Design a combinational logic circuit for the full-subtractor with the help of a truth table and Karnaugh map.

ii. Design a modulo-13 ripple counter using negative edge triggered JK flip-flop.