13-12-2017

03:00 pm - 06:00 pm

DIGITAL LOGIC DESIGN AND ANALYSIS **Q.P. Code: 24867**

(3 Hours) **[Max. Marks 80]**

N.B

1. **Question no. 1 is compulsory.**
2. **Attempt any 3 from the remaining questions.**
3. **Assume suitable data if necessary.**
4. **Figures to right indicate full marks.**

Q 1 (a)	Prove using Boolean algebra: "NAND gate is Universal gate"	**05**
Q 1 (b)	A 7-bit even parity hamming code is received as 1000010. Correct it for any errors and extract 4 bit data	**05**
Q 1(c)	Simplify $F(P,Q,R,S) = \pi M(3,4,5,6,7,10,11,15)$ using kmap and implement using minimum number of gates.	**05**
Q 1(d)	Explain Johnson Ring Counter	**05**
Q 2(a)	Reduce equation using Quine McCluskey method and realize circuit using basic gates– $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + d(2,4)$	**10**
Q 2(b)	Compare TTL and CMOS wrt to gate, voltage level, fan in fan out, propagation delay	**10**
Q 3 (a)	What is race around condition? How to overcome it?	**10**
Q 3 (b)	Implement full subtractor using basic gates	**10**
Q 4(a)	Design a 32:1 multiplexer using 4:1 multiplexer with suitable diagrams and tables	**10**
Q 4 (b)	Explain 3 bit asynchronous down counter with timing diagram and truth table	**10**
Q 5(a)	Explain the working of 4-bit parallel adder. Identify its disadvantage how to overcome it?	**10**
Q 5(b)	Convert SR flipflop to D flipflop.	**10**
Q 6	Write short note on **(any 4)**	**20**

1) VHDL
2) 4 bit magnitude Comparator
3) Pseudo random number generator
4) Universal Shift Register
5) ALU

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