University of Mumbai

Examination 2022

Program No. & Name of the Examination: 1T00724 / S.E. (Computer Engineering)(SEM-IV)(Choice Base Credit Grading System)(R2016)

Course Name: Computer Organization and Architecture

Subject Code: CSC403

Paper code: 40503 Max. Marks: 80

For the students: All the Questions are compulsory and carry equal marks.

Q1: Answer the correct option. (20 M)

Q1.	In IEEE floating point representation, the Hexadecimal number 0XC0000000 corresponds to..
Option A:	-3.0
Option B:	-1.0
Option C:	-2.0
Option D:	-4.0
Q2.	Which of the following is used for binary multiplication?
Option A:	Restoring Multiplication
Option B:	Booth's Algorithm
Option C:	Pascal's Rule
Option D:	Digit-by-digit multiplication
Q3.	In microprocessor the Instruction Cycle (IC), Fetch Cycle (FC) and Execution Cycle (EC) are related as
Option A:	IC = FC-EC
Option B:	FC=EC+IC
Option C:	IC = FC+EC
Option D:	EC = IC+FC
Q4.	One instruction tries to write an operand before it is written by previous instruction. This may leads to a dependency called..
Option A:	True dependency
Option B:	Anti-dependency
Option C:	Output dependency
Option D:	Control hazard
Q5.	The main difference between a CISC and RISC processors is/are that a CISC processors has a
Option A:	A smaller no of microinstructions
Option B:	Fixed length instruction format
Option C:	Fewer addressing modes
Option D:	Less registers
Q6.	A register of microprocessor that stores the result of ALU operation is …..
Option A:	Stack Pointer

Option B:	Instruction Pointer
Option C:	Flag Register
Option D:	Accumulator
Q7.	If the page no. is not found in TLB, Then, it is known as
Option A:	Page fault
Option B:	TLB miss
Option C:	TLB hit
Option D:	Cache miss
Q8.	In segmentation, each address is specified by
Option A:	a segment number & offset
Option B:	an offset & value
Option C:	a value & segment number
Option D:	a key & value
Q9.	Which of the following is not true about cache memory
Option A:	Faster memory than RAM
Option B:	Volatile memory
Option C:	Smaller in size than RAM
Option D:	Sequential access memory
Q10.	DMA transfers data between-------
Option A:	Memory and processor.
Option B:	Processor and I/O devices.
Option C:	I/O devices and memory.
Option D:	DMA and Memory

Q2	**Solve any four out of five (20 marks)** **05 marks each**
A	What is the role of MAR and MDR?
B	Explain floating point representation.
C	Compare hardwired and microprogrammed control units.
D	Write shot note on superscalar architecture.
E	Explain Flynn's Classification

Q3	**Solve any Two out of Three (20 marks)** **10 marks each**
A	Explain direct and set associative mapping techniques in cache.
B	What are the instruction pipeline? What are the conflicts that occurred during instruction pipeline?
C	Explain Booth's algorithm with example

Q4	Solve any Two out of Three (20 marks) 10 marks each
A	State various types of data transfer techniques. Explain DMA data transfer in detail.
B	Explain multicore processor architecture with block diagram.
C	Explain in details Bus arbitration techniques.