

Duration: 3hrs

[Max Marks: 80]

- N.B. :** (1) Question No 1 is Compulsory.
 (2) Attempt any three questions out of the remaining five.
 (3) All questions carry equal marks.
 (4) Assume suitable data, if required, and state it clearly.

- 1 Attempt **any FOUR** [20]
 - a Differentiate between CPLD and FPGA.
 - b Differentiate between SRAM and DRAM memories.
 - c Differentiate between TTL and CMOS logic families.
 - d Write a short note on VHDL.
 - e State and explain DeMorgan's theorem.
- 2 a Implement Ex-OR and Ex-NOR gates using NAND and NOR gates with necessary proof. [10]
 - b Design full subtractor and implement using logic gates. [10]
- 3 a Explain 4bit Johnson counter with neat diagram and waveforms. [10]
 - b $F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$. Reduce using Quine Mc Cluskey method. [10]
- 4 a Design full adder using 4:1 multiplexer. [10]
 - b Subtract 14 from 24 using 1's and 2's complement method. [10]
- 5 a Explain race around condition. Explain with diagram master slave JK flip flop. [10]
 - b Design 2 bit comparator and implement using logic gates. [10]
- 6 a Differentiate between VHDL modeling styles: data flow, behavioural and structural. [5]
 - b Differentiate between PROM, PAL, PLA. [5]
 - c Design Mod-6 Synchronous up counter. [10]
