Date -22/11/19

Paper / Subject Code: 49304 / DIGITAL LOGIC DESIGN AND ANALYSIS

S.E. (Computer) (Sem-III) (CBSGS) (R-2012)

Time: 3 Hours **Total Marks: 80**

N.B. (1) Question No. 1 is compulsory
(2)Assume suitable data if necessary
(3)Attempt any three questions from remaining questions

1 Attempt any 5

(a) Convert $(216.24)_{10}$ into octal, binary and hexadecimal, and base 4. (4)
(b) perform $(76)_{10} - (33)_{10}$ in BCD using 10's complement method (4)
(c) Explain Glitch problem. (4)
(d) State De Morgan's theorem. Prove NAND is Universal gate. (4)
(e) Encode the data bits 110010001 using Hamming code. (4)
(f) Explain SOP and POS and solve the following using K-Map
$F(A,B,C,D)=\sum m(1,5,6,7,10,11,13)+d(2,4)$ (4)
(g) Explain parity generator/checker. (4)

2 (a) Reduce equation in SOP form using Quine McCluskey method and realize circuit using basic gates. $F(A,B,C,D) = \pi M(2,7,8,9,10,12)$ (10)
(b) Explain and Design a BCD adder using 4 bit binary adders. (10)

3 (a) Implement 16:1 Mux using 8:1 Mux. (5)
(b) Explain lockout condition. How can it be avoided. (5)
(c) Design a 2 bit magnitude comparator. (10)

4 (a)Explain with neat diagram 2 input TTL NAND gate in detail. (10)
(b) Explain 4 bit bidirectional shift register. (10)

5 (a) Design mod 10 asynchronous counter using T flipflop (10)
(b) Convert SR flipflop to JK flipflop and T flipflop. (10)

6 Write short note on (any two):- (20)
(a) 3 bit Up/Down Asynchronous Counter
(b) 4-bit Universal shift register
(c) VHDL

163A4613477425A40D6893384417A4FD