University of Mumbai

Examinations Summer 2022

Program: Electronics and Telecommunication Engineering

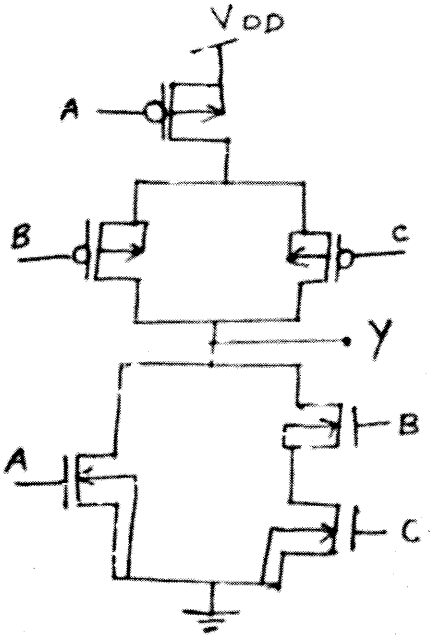
Curriculum Scheme: Rev2016

Examination: TE Semester VI

Course Code: ECCDLO6021 and Course Name: Digital VLSI Design

Time: 2 hour 30 minutes Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	In a NOR based ROM, data bit '1' is stored using,
Option A:	Absence of a transistor
Option B:	Presence of a transistor
Option C:	Series combination of transistor
Option D:	Parallel combination of transistor
2.	The output of 8X4 barrel shifter after performing 3 bit logical left shift operation on 11010111
Option A:	1101
Option B:	0101
Option C:	1011
Option D:	0111
3.	Which of the following statement is not true?
Option A:	Two metal lines can cross each other at the same layer
Option B:	When a polysilicon crosses a diffusion region, it represents a MOSFET
Option C:	Stick diagrams do not represent dimensions of MOSFET
Option D:	Stick diagrams do not represent parasitic in the circuit
4.	Which method of physical clocking is a recursive structure where the memory elements are grouped together to make the use of nearby or same distribution points?
Option A:	Clock skew
Option B:	Balanced tree clock network
Option C:	H tree
Option D:	Single phase two level clocking
5.	In a NMOS Pass transistor the maximum output voltage possible is
Option A:	V_{DD}
Option B:	$V_{DD} + \|V_{T0n}\|$
Option C:	$V_G + \|V_{T0n}\|$
Option D:	$\|V_{T0p}\|$
6.	The transistors in NAND type flash are connected in
Option A:	series
Option B:	parallel
Option C:	cascade
Option D:	cascode

7.	The power consumption of a dynamic RAM is
Option A:	More than that of static RAM
Option B:	Equal to that of a static RAM
Option C:	Less than that of a static RAM
Option D:	Zero
8.	What is the logic equation of the given circuit? 
Option A:	$Y = \overline{A + B(C + D)}$
Option B:	$Y = \overline{A + BC}$
Option C:	$Y = \overline{A(B + C) + D}$
Option D:	$Y = \overline{AB + C}$
9.	How does controller FSM differ from HLSM
Option A:	FSM have fewer states than HLSM
Option B:	Condition for state transition in FSM is a signal status, whereas HLSM have logical condition
Option C:	FSM do not have external control inputs, HLSM have external control inputs
Option D:	In FSM state transition can happen without an event, in HLSM the transition can happen only on the occurrence of an event
10.	Look up table is basic unit in which of the following technology
Option A:	ASIC
Option B:	PLA
Option C:	CPLD
Option D:	FPGA

Q2	**Solve any Two** **10 marks each**
A	Draw layout of 6-T SRAM cell and Describe working of FLASH memory

B	Explain the concept of strong and weak logic in pass transistors. Draw a 4:1 Mux in NMOS pass transistor logic, PMOS pass transistor logic and Transmission gate logic.
C	Design Parallel 3-TAP FIR filter using RTL design technique. Draw HLSM, Datapath, Interface and Controller FSM. Compare it with Serial FIR filter

Q3		
A	**Solve any Two**	**5 marks each**
i.	Write a short note on ESD protection	
ii.	Explain with diagram working of 3-T DRAM and 1-T DRAM. Compare these designs	
iii.	Write a short note on Input and Output Circuits	
B	**Solve any One**	**10 marks each**
i.	Implement $Y = AB + BC + CA$ using a) Static CMOS logic b) NORA chain c) Domino Chain. d) Dynamic PMOS	
ii.	Draw layout of clocked JK latch and write HDL program D-Flip Flop	

Q4		
A	**Solve any Two**	**5 marks each**
i.	Write a short note on Charge sharing	
ii.	Design circuit for 4 bit array multiplier	
iii.	Compare HLSM and FSM	
B	**Solve any One**	**10 marks each**
i.	Design RTL for Sum of absolute differences using RTL design technique. Draw HLSM, Datapath and FSM.	
ii.	Design a 3- bit carry generator block of carry look ahead adder using Dynamic N-MOS design style. Write a HDL program for 3-BIT carry look ahead adder	