

Time: 3 Hours

Marks: 80

- N.B.: (1) Question No. 1 is compulsory.
 (2) Solve any three questions from the remaining five questions.
 (3) Figures to the right indicate full marks.
 (4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions

[20]

- Explain various types of capacitors.
- Why should collector resistor R_C be as large as possible in the design of CE amplifier?
- Explain Zener as voltage regulator.
- State and explain Miller's Theorem.
- Draw and explain small signal model of a diode.
- Explain the hybrid pi model of BJT.

Q.2 (a) Explain the fabrication steps of passive elements.

[5]

(b) Explain concept of zero temperature drift in JFET.

[5]

(c) Design an L section LC filter with full wave rectifier to meet the following specifications: The DC output voltage $V_{DC} = 220$ V deliver $I_L = (70 \pm 20)$ mA to the resistive load and the required ripple factor is 0.04.

[10]

Q.3 (a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h parameters?

[10]

(b) Determine I_{DQ} , V_{GSQ} , V_{DSQ} if $I_{DSS} = 9$ mA and $V_p = -3$ V for the circuit given in Fig. 3(b).

[10]

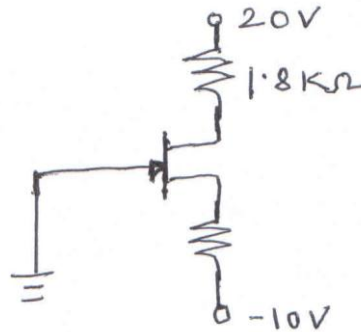


Fig. 3(b)

Q.4 (a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6)$ mA and $|A_v| = 12$.

[10]

(b) For the circuit shown below in Fig.4(b), the transistor parameters are $V_{BE(on)} = 0.7$ V, $\beta = 200$ and $V_A = \infty$.

 V_{BE}

[10]

- Derive the expression for lower cut-off frequency (or time constant) due to input coupling capacitor.
- Determine lower cut-off frequency and midband voltage gain.

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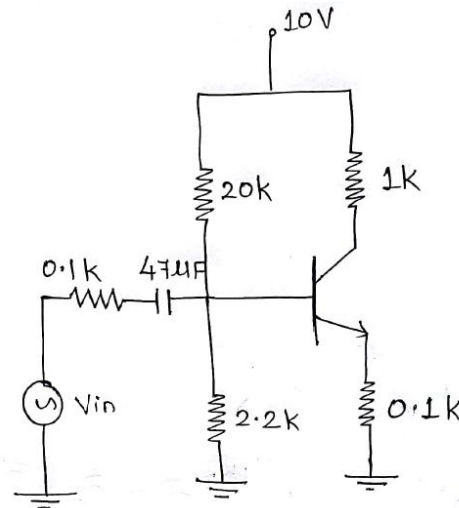


Fig. 4(b)

- Q.5 (a) For the circuit using JFET as shown in Fig. 5(a), if $I_{DSS} = 6 \text{ mA}$, $V_p = -6 \text{ V}$, $r_d = \infty$, $C_{gd} = 4 \text{ pF}$, $C_{gs} = 6 \text{ pF}$, $C_{ds} = 1 \text{ pF}$, Determine i) V_{GSQ} , ii) I_{DQ} , iii) g_{mo} , and iv) g_m . [10]

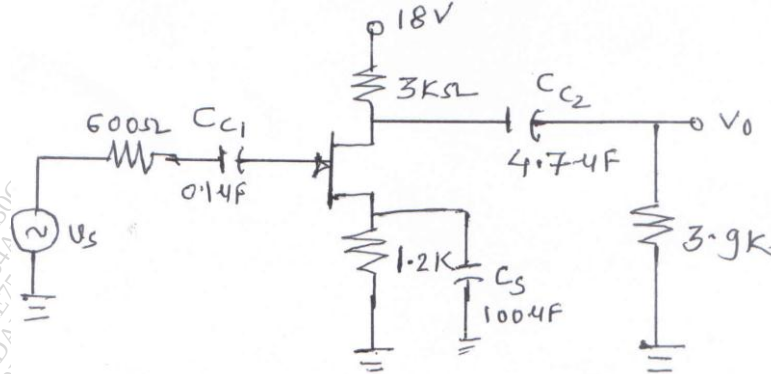


Fig. 5(a)

- (b) For the circuit shown below in Fig. 5(b), the transistor parameters are $V_{BE(on)} = 0.7 \text{ V}$, $\beta = 100$ and $V_A = \infty$. Determine Z_i , Z_o and A_v . [10]

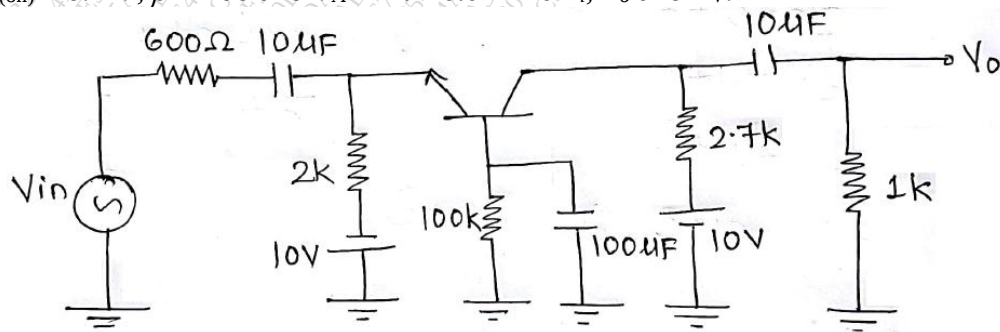


Fig. 5(b)

- Q.6 Short notes on: (Attempt any four) [20]

- High frequency π equivalent model of common emitter BJT.
- Stability factors of various biasing techniques of BJT.
- Comparison of BJT CE and JFET CS amplifier.
- Different types of filters.
- JFET parameters.

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