(3 Hours) **Marks: 80**

Note the following instructions.

1. **Question No.1 is compulsory**
2. **Attempt any three questions from remaining five questions**
3. **Solve in total 4 questions**
4. **Assume suitable data wherever necessary, justify the same**
5. **Figures to the right indicate full marks.**

1.a Draw the state diagram and state table to detect 1010 overlapping sequence using Melay type model. **[5]**

1.b Explain why an X-OR gate cannot be implemented by using single threshold gate. **[5]**

1.c Reduce the following expression using 4 variable Kmap. **[5]**

$U = Em_3 + m_5 + m_7 + Fm_{10} + m_{12} + m_{14}$

1.d Find the state equivalence partition and corresponding reduced machine in standard format **[5]**

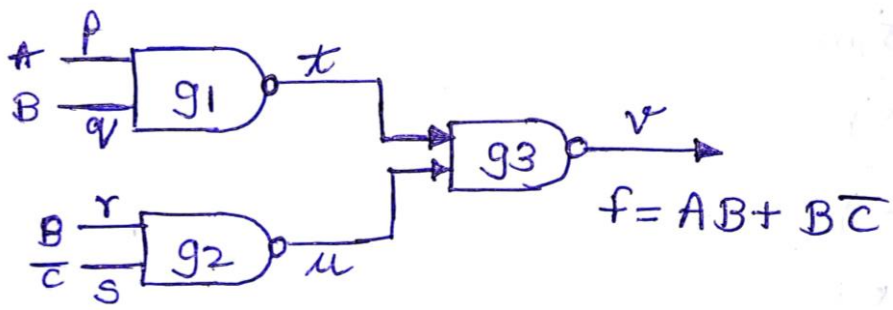
Present State	Next State, Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

2.a Minimize the following expressions using Quine McCluskey method. **[10]**

$F(X1,X2,X3,X4) = \sum m(0,1,2,8,9,15,17,21,24,25,27,31)$

2.b For the given circuit shown below, **[10]**

i. construct a fault table
ii. determine minimal fault detection test
iii. develop a fault location test and construct a fault library for each circuit.



3.a Check the following Boolean function for unatenes and realise using T-gate. **[10]**

$$F(U,V,W,X)= \sum m(4,5,8,9,11,12,13,14,15)$$

3.b Find the homing sequence and synchronizing sequence for the following machine. **[10]**

Present State	Next State, Z	
	X=0	X=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

4.a Design a Melay type synchronous sequential circuit using memory element for the following problem. The machine should have two input terminals designated X1 and X2, which carries two binary numbers to be add serially. One output terminal designated Z to represent the sum. The inputs and outputs should have fixed length sequences of 0's and 1's. **[10]**

4.b With a suitable example explain what is path sensitisation and how it can be used to determine tests to detect faults in circuit **[10]**

5.a For state tables of the incompletely specified sequential machines given below, find the set of maximal compatibles using (a) Merger Graph method (b) Merger Table method **[10]**

Present State	Next State, Z			
	00	01	11	10
A	A,-	-,-	F,-	C,1
B	F,-	B,1	C,-	-,-
C	-,-	C,0	-,1	D,0
D	A,0	-,-	E,1	C,-
E	C,0	-,-	C,0	-,-
F	-,-	B,1	-,0	B,1

5.b Design a datapath subsystem for binary multiplier using add shift algorithm. Draw the Algorithmic State Machine chart for the same. **[10]**

6.a. What are Melay and Moore finite state machine? Compare them **[5]**

6.b. Describe and ASM chart and explain it's importance in hardware design **[5]**

6. c. What is a logic hazard and describe in brief the types of logic hazard. **[5]**

6 d. Mention the different types of faults present in logic circuits and list the method to detect and locate them. **[5]**