feb-2023

S.E.(EXTC) (Sem-III) (CBCGS) (R-20-21) (C Scheme

Time: 3 hour **Max marks 80**

N.B.: (1) Question 1 is compulsory.
(2) Attempt any 3 out of remaining 5 questions
(3) Assume suitable data if required.
(4) Figures to the right indicate full marks.

Q1. **Solve any four**

a) Prove that NAND and NOR are universal gates **05**

b) Why and which code is used for labelling the cells of K-map **05**

c) Perform the following operation using 2's complement method **05**
(i) $(7)_{10}$-$(15)_{10}$ **(ii)** $(50)_{10}$-$(2A)_{16}$

d) Write a VHDL code for 4-bit adder **05**

e) What is Race around condition in JK FF how to overcome it **05**

Q 2 **Solve the following**

a) Convert SR flip flop to JK Flip flop **10**

b) Minimize the following function using Quine MC-Cluskey **10**
$f(A, B, C, D) = \sum m(1,3,7,11,15) + d(0,2,5)$

Q 3 **Solve the following**

a) Using Boolean algebra prove the following
i) $AB+BC+A\bar{C}=AB+A\bar{C}$ **10**
ii) $[(C+\bar{C}D)(C+\bar{C}\bar{D})][AB+A\bar{B}+(A \text{ XOR } B)]=C$

b) Convert following **to** decimal **10**
(i) $(352.7)_8$ **(ii)** $(458.54)_8$

Q .4 **Solve the following**

a) What is shift register? Explain anyone type of shift register give its applications **10**

b) Design two-bit comparator and implement using logic gates **10**

Q 5 **Solve the following**

a) Design 3 bit binary to Gray code converter circuit using logic gates **10**

b) Draw and explain a neat circuit diagram of BCD adder using IC 7483 **10**

Q.6. **Solve the following**

a) Compare PAL with PLA **05**

b) Represent the following by Boolean expression by min/max terms. **05**
$Y(A,B,C,D)=(A+B+\bar{C})(\bar{A}+C+\bar{D})$

c) Design Full adder circuit using PLA **10**

Q.P.Code:10020818

Please read as

Q.3) a) i) $AB + BC + \bar{A}C = AB + \bar{A}C$

ii) $[(C + \bar{C}D)(C + \bar{C}\bar{D})][AB + \bar{A}\bar{B} + (A\ ExOR\ B)] = C$

Q.3)b) ii) $(457.54)_8$