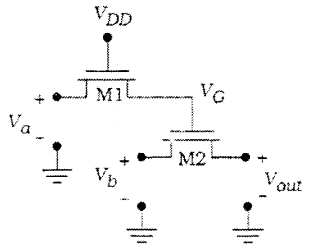
T.E. (EXTC) (Sem-VI) (CBSGS)

Paper / Subject Code: 37006 / VLSI DESIGN Date-18/12/19

Time: 3 Hours **Marks: 80**

N.B: (1) Question No 1 is compulsory. Solve any three from the remaining five questions
(2) Figures to right indicate full marks
(3) Assume suitable data if necessary and mention the same in the answer sheet

1. Solve the following 20M
   a. Implement 4:1 Mux using Transmission Gate.
   b. Explain charge sharing in detail with proper diagram
   c. Explain different CMOS clock generation methods
   d. For following circuit diagram Vdd = 3.3V, Vt =0.6 V Find Vout for
      1) Va = Vb = 3.3 V and (2) Va = 0.5 V Vb = 3 V



   e. Draw 6T SRAM cell

2A. Explain the process of nMOS fabrication with the help of neat sketches along with the masks required 10M

2B. Draw 4x4 bit NOR based ROM array to store the following data in respective memory locations 10M

Memory Address	Data
0001	0011
0010	1101
0100	0110
1000	1101

3A. Implement $Y = \overline{(k + lm)np}$ using any 4 of the following design styles 10M
   I. Dynamic pMOS array
   II. Dynamic nMOS Array
   III. Domino Gate
   IV. Static CMOS
   V. Pseudo nMOS

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3B. Implement CMOS Clocked JK latch and draw layout using lambda rules 10M

4A. Consider CMOS inverter circuit with following parameters $V_{dd} = 3.3V$, $k_r = 2.5$, $k_n = \frac{200\mu A}{V^2}$, $k_p = \frac{80\ \mu A}{V^2}$, $V_{T0n} = 0.6V$, $V_{T0p} = -0.7V$ calculate the critical voltages $V_{OL}, V_{OH}, V_{IL}, V_{IH}$ and the noise margin of the circuit. Note inverter is not symmetric. 10M

4B. For CMOS inverter derive VIL,VOH,VIH and VOL. also Find Noise margin 10M

5A. Draw circuits for the following using CMOS 10M

i. Carry Circuit of 4-Bit CLA adder using Dynamic NMOS

ii. 1-BIT Full adder (Hint - 28 transistors circuits)

5B. Draw and explain 4-bit carry save multiplier with neat diagram 10M

6A. Draw the CMOS circuit for $Y = \overline{A + DE + F}$ and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that *(W/L)* = 10 for all pMOS transistors and *(W/L)* = 15 for all nMOS transistors. 10M

6B. Write brief notes on any 2 of the following 10M

I. Clocking methods

II. Clock distribution

III. Short channel effects

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