Paper / Subject Code: 42457 / CMOS Mixed Signal VLSI (DLO)

B.E. (EXTC) (Sem - VII) (CBS) Date - 22/11/19

Time : 3 Hours **Marks : 80**

N. B. : (1) Question No. 1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

Q.1 A. Explain active current mirror circuits. 5 Marks
B. Derived expression for input referred noise of CS stage. 5 Marks
C. Explain Ring oscillator. 5 Marks
D. Explain concept of switched capacitor circuits. 5 Marks

Q.2 A. Derived expression for voltage gain AV and Output resistance Ro of source follower stage. 10 Marks
B. Explain simple PLL-phase detector. What are the Non ideal effect inPLL. 10 Marks

Q.3 A. Explain the charge injection mechanism in MOS sampling circuits and also describe 10 Marks
B. Explain the concept of switch capacitor circuits. Analyse 2nd order switched capacitor circuits 10 Marks

Q.4 A. Derived equations of differential gain, common mode gain and CMRR of differential amplifier circuits. 10 Marks
B. What is a band gap reference? Describe methods of implementation of band gap references. 10 Marks

Q.5 A. Explain ADC architecture. What is 2-step flash ADC. 10 Marks
B. What are the different issue in analog mixed-signal CMOS integrated circuits. 10 Marks

Q.6 A. Cyclic Data converter architecture (DAC). 5 Marks
B. Successive approximation ADC. 5 Marks
C. Voltage controlled oscillator (VCO). 5 Marks
D. Widlar current mirror. 5 Marks

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