Q.P. Code: 40879

(80 Marks) **(3 Hours)**

- Question no. 1 is compulsory.
- Answer any three questions from question no. 2 – 6.
- Assume suitable data, if necessary.

Q.1. Answer following questions in brief.

	a	Convert the following number 256.325 into IEEE 32 bit Single Precision Format and IEEE 64 bit Double Precision Format	**(05)**
	b	Discuss difference between RISC and CISC processors.	**(05)**
	c	Explain function of 8089 I/O processor in brief.	**(05)**
	d	Differentiate between SRAM and DRAM	**(05)**
Q.2.	a.	Explain cache consistency and coherency with suitable examples. Also, give methods to maintain cache consistency.	**(10)**
	b.	Explain DMA based data transfer techniques.	**(10)**
Q.3.	a.	Explain how Virtual Address is translated to Physical address with suitable example.	**(10)**
	b.	Compare between Cache Look Aside Architecture and Cache Look through Architecture	**(10)**
Q.4.	a.	Explain the Bus Arbitration Techniques	**(08)**
	b.	Explain hardwired Control Unit with help of neat diagram. Compare it with microprogrammed control unit.	**(12)**
Q.5.	a.	What is TLB? Explain working of TLB.	**(10)**
	b.	Describe register organization within CPU.	**(10)**

Q.6. Write short note on

a.	Hazards in Pipelining	**(05)**
b.	Interrupt driven I/O	**(05)**
c.	Interleaved memory	**(05)**
d.	Modes of DMA	**(05)**

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